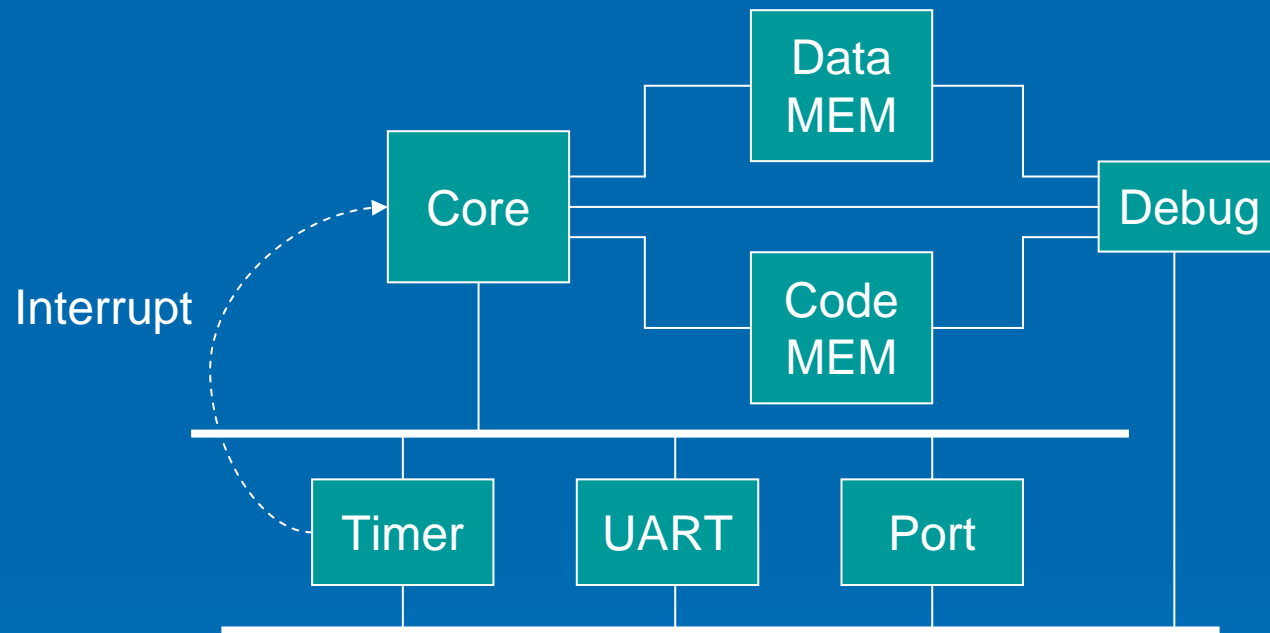


Design of a multi-core time-triggered microprocessor

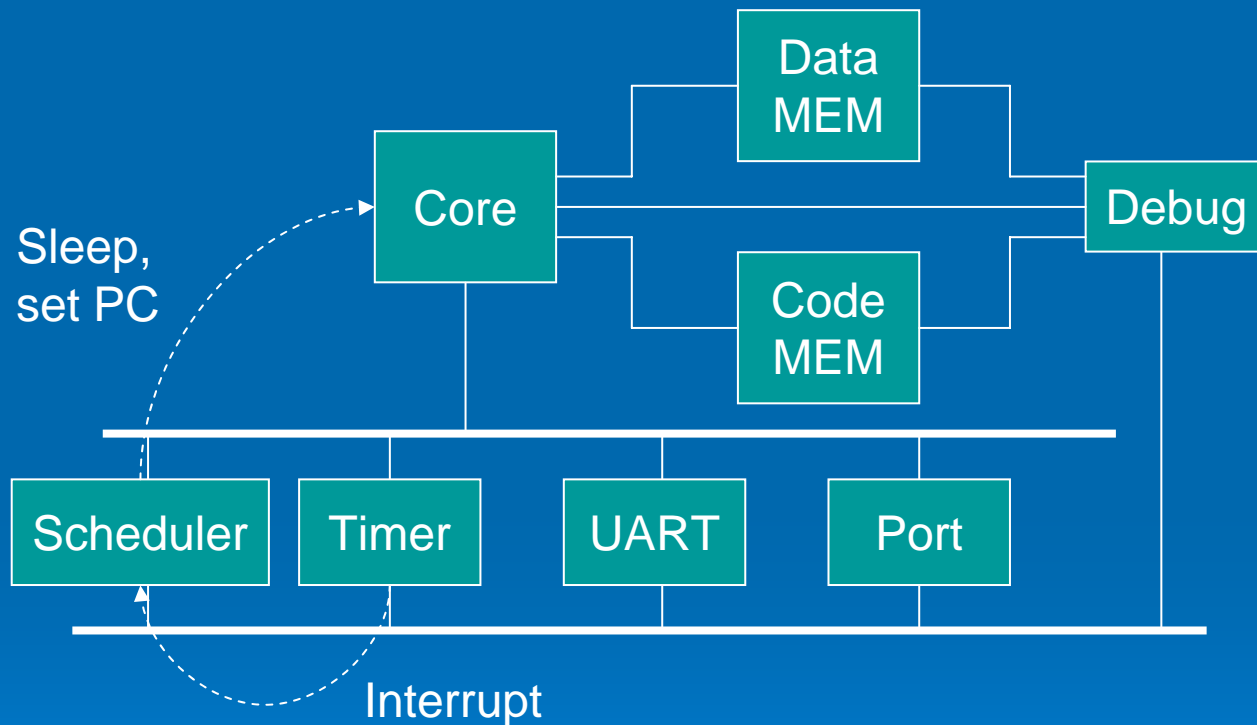
ESL Seminar – Keith Athaide



Single-core PH processor

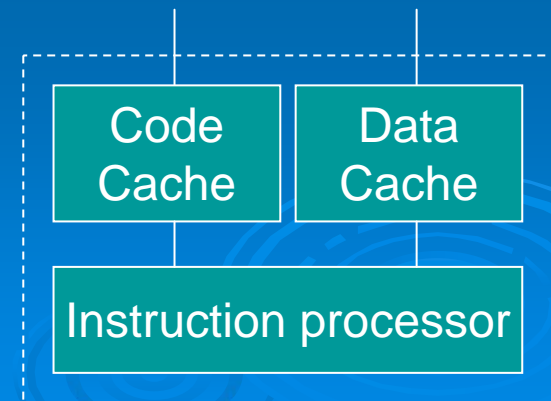
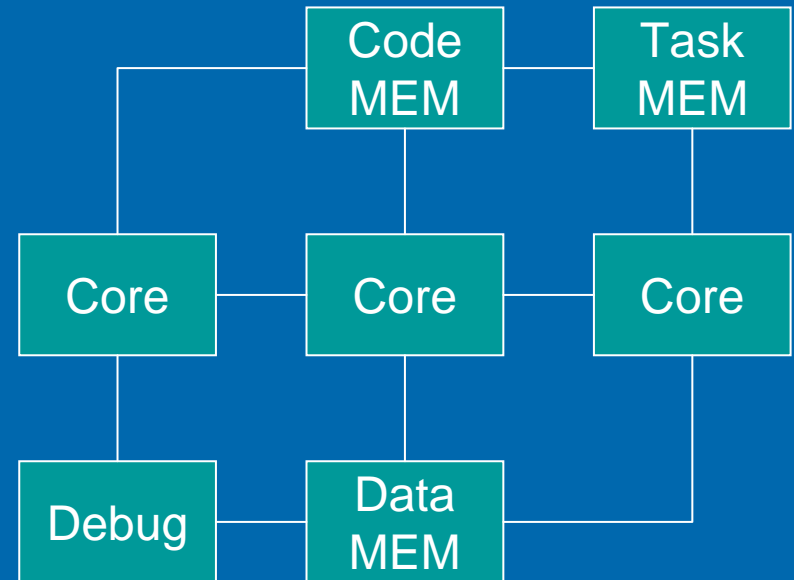


Single-core PH processor with hardware TTC scheduler



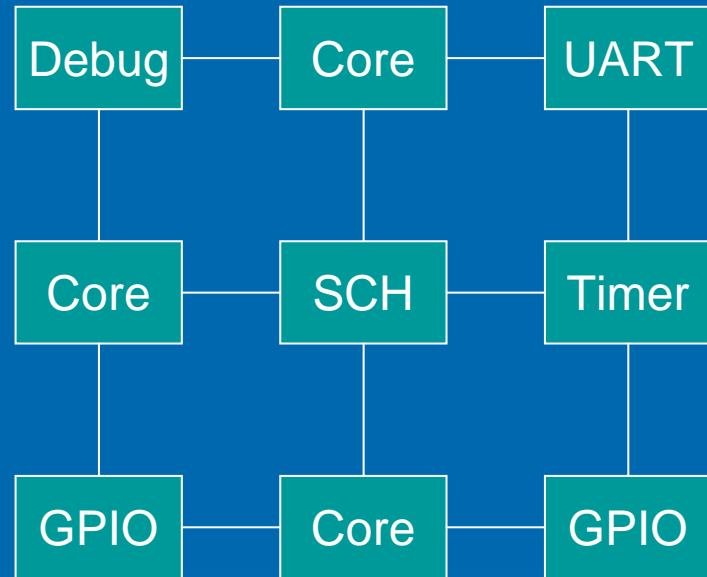
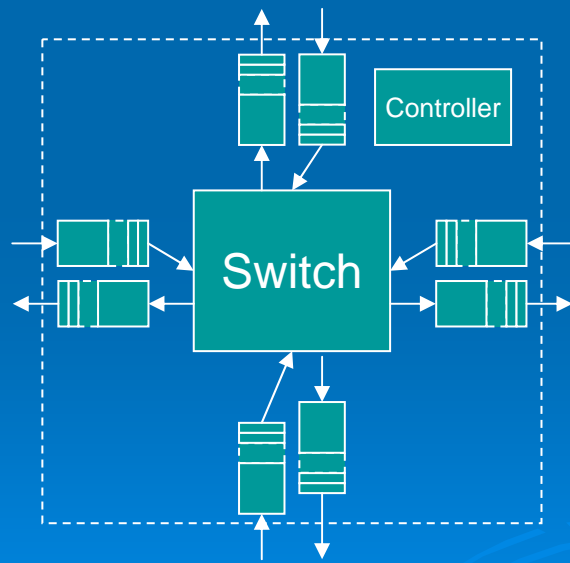
Memory network

- Task memory
 - Smaller
 - On-chip
 - Values not cached
- Caches introduced
 - request from the correct node
- Loads and stores block
- No cache coherence scheme



IP core network

- Mesh topology
- Memory mapped communication



```
#define SCHCON (*((volatile  
                unsigned long *) 0x00030000))  
  
SCHCON = 0x1;
```

Start-up procedure

Core 1

```
$gp = 0x1000  
$sp = 0x107f0  
# Clear BSS  
# Setup scheduler  
# Start scheduler  
sleep
```

Core 2

```
$gp = 0x1000  
$sp = 0x117f0  
sleep
```

Core 3

```
$gp = 0x1000  
$sp = 0x127f0  
sleep
```

Simulation

- Fast cycle-accurate simulation
 - GT 25,000,000 cycles in 1 second
- Trialled implementations
 - RTL translation
 - Direct VHDL to C++
 - SystemC
 - Higher level abstraction
 - C++
 - Minimized use of polymorphism, RTTI

Versions

- Single-core
- Single-core with scheduler
- Single-core with scheduler and caches
 - Was able to extract hit and miss rates

Simulator screenshot

The screenshot displays the RapidTTy simulator interface, which is used for developing and debugging embedded systems. The interface is divided into several panels:

- Debug Panel:** Shows the current execution state, including the PH Processor, GDB Server (Suspended), Thread [0] (Suspended), and the main thread at `main.c:46`. It also indicates that the code upload was successful and terminated with an exit value of 0.
- Variables Panel:** Displays a table of variables and their values:

Name	Value
Processor time	0.000 054 560 s
Processor cycles	1,364
Time between breakpoints	0.000 001 920 s
Breakpoint ISR execution time	0.000 000 480 s
Minimum	0.000 000 480 s
Maximum	0.000 000 480 s
Range	0.000 000 000 s
Average	0.000 000 480 s
- Tasks Panel:** Shows a table of tasks and their periods:

I.	Name	D...	Period
0	Elapsed_Time_UART0_U...	1	1000
1	UART0_O_Update	1	10
- Code Editor:** Displays the source code for `main.c`, showing the initialization of the scheduler and the start of a super loop:

```
Elapsed_Time_UART0_Init();  
  
// Add tasks to the scheduler  
SCH_TTC_Add_Task(Elapsed_Time_UART0_Update, 0, UART0_O_Update);  
SCH_TTC_Add_Task(LED_Update, 0, LED_BLINK);  
  
// Start the scheduler  
SCH_TTC_Start();  
  
while (1) // Super Loop  
{  
    // ...  
}
```
- Peripherals Panel:** Configures hardware components:
 - Timer 0:** TOCON is 0, EN is unchecked, Duration is 1 ms, Prescaler is 18, TOVAL is 3e7, TOREL is 3e7.
 - Uart 0:** Pin numbers are Output: 11, Input: 20, Input/Output: 1.
 - Port 0:** IOPIN0 is configured with pins 7, 15, and 8.
- Console:** Shows the current output, including the status of the RS232 - VIR1 interface and the PH/TTEC datapath.