The Application of Dynamic Voltage Scaling in Embedded Systems Employing A TTCS Software Architecture

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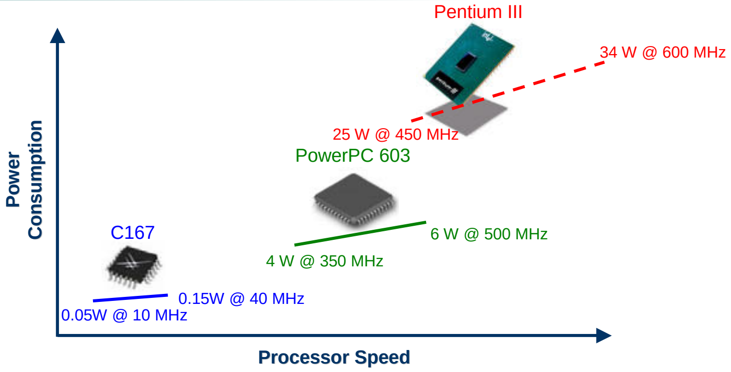
Motivation



- Mobile systems have limited (battery) life.
- How can we extend the system's life?

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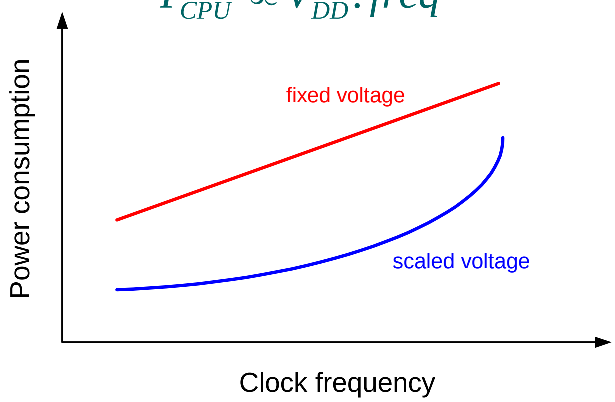
Overview

- In this talk, I will consider ways in which we can reduce CPU power consumption, allowing us to extend the system life of mobile embedded systems
- I will consider how we can implement “Dynamic Voltage Scaling” (DVS) techniques in systems with a “Time-Triggered, Co-operatively Scheduling” (TTCS) architecture
- I will then compare the power-saving efficiency of DVS and TTC scheduling algorithms

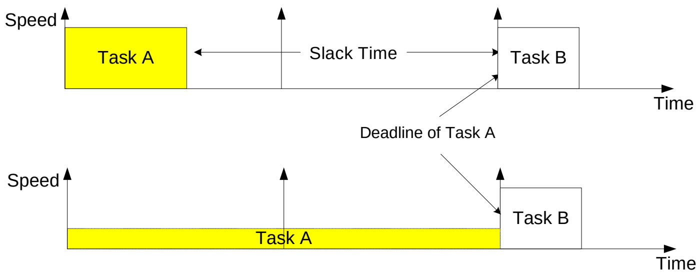
Power consumption in CMOS processors

$$P_{CPU} \propto V_{DD}^2 . freq$$



DVS in TTCS designs

- Balancing power consumption and performance by employing “Dynamic Voltage Scaling”



Note: Varying speed means supply voltage also adjusted

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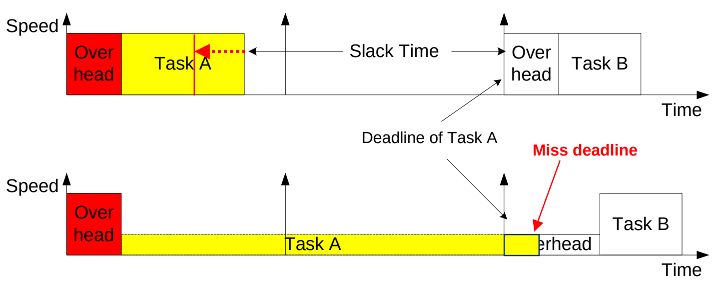
Realistic DVS implementation

- DVS scheduling overhead (task Scheduling, PLL locking, voltage scaling, speed finding calculation) is large
- **How much power (if any) does DVS save?**



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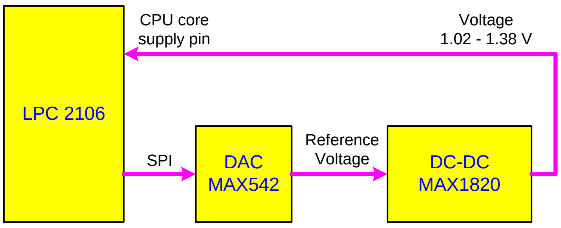
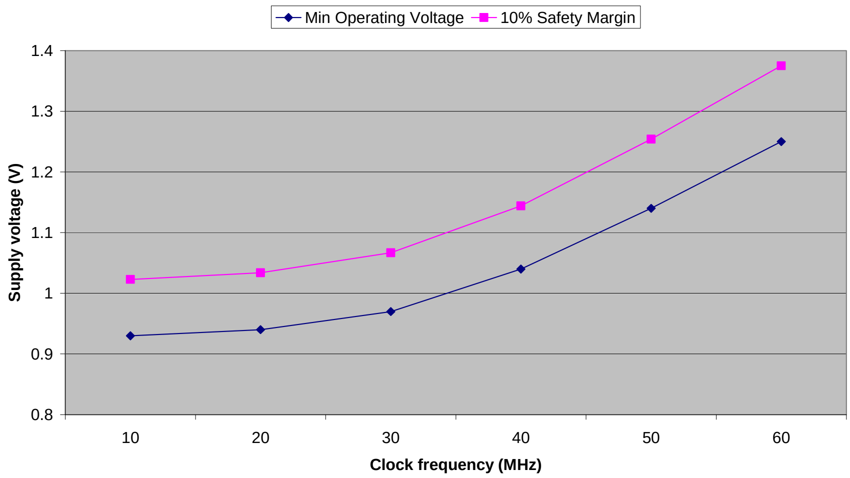
The hardware platform

- Philips LPC2106: 32-bit microcontroller with an ARM7-core
- Ashling EVBA7 evaluation board
- Clock frequency: 10-60 MHz



A DVS schematic diagram

CPU core supply voltage setting

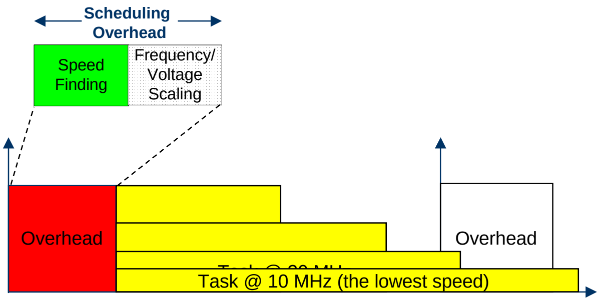


Scheduling algorithm development

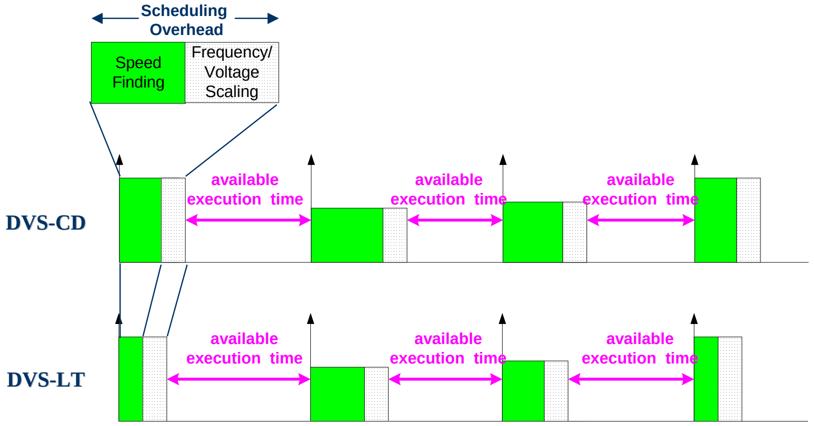
- DVS Scheduling algorithms based on TTCS
  - Compute Direct (DVS-CD)
  - Lookup Table (DVS-LT)
  - Circular Array (DVS-CA)
  - Circular Skip (DVS-CS)
- The main aim is to reduce the scheduling overhead

DVS algorithms

- Speed-finding procedure will seek the optimal speed to complete a task before its deadline
- Voltage/Frequency scaling procedure will adjust operating frequency and supply voltage corresponding to the assigned speed

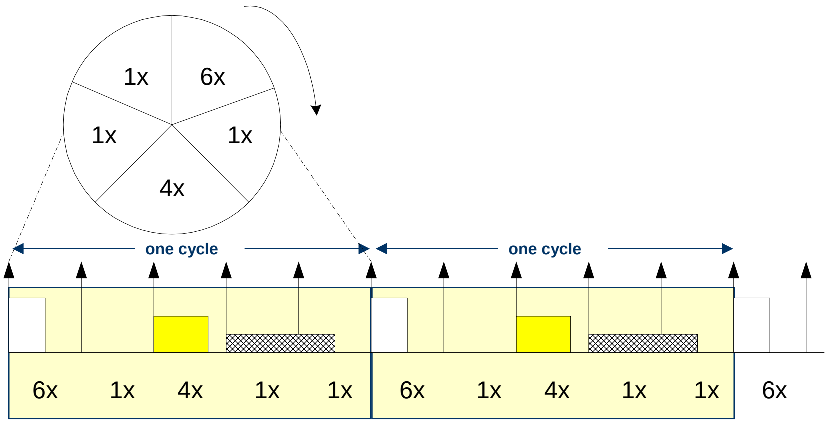


DVS algorithms (2)

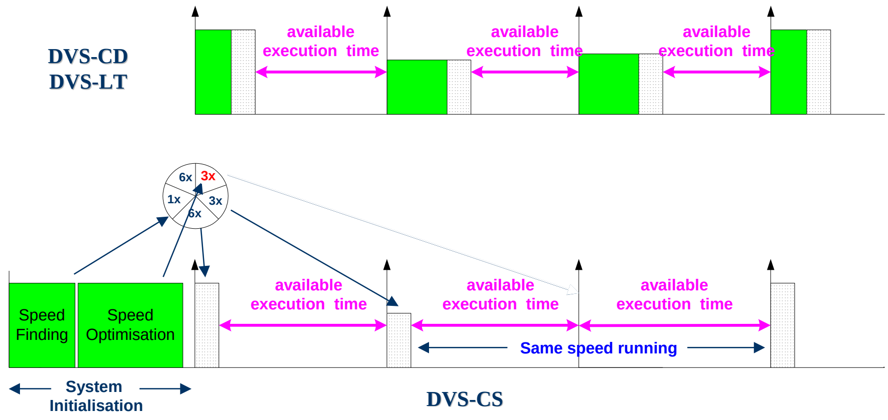


DVS algorithms (3)

Circular Array



DVS algorithms (4)



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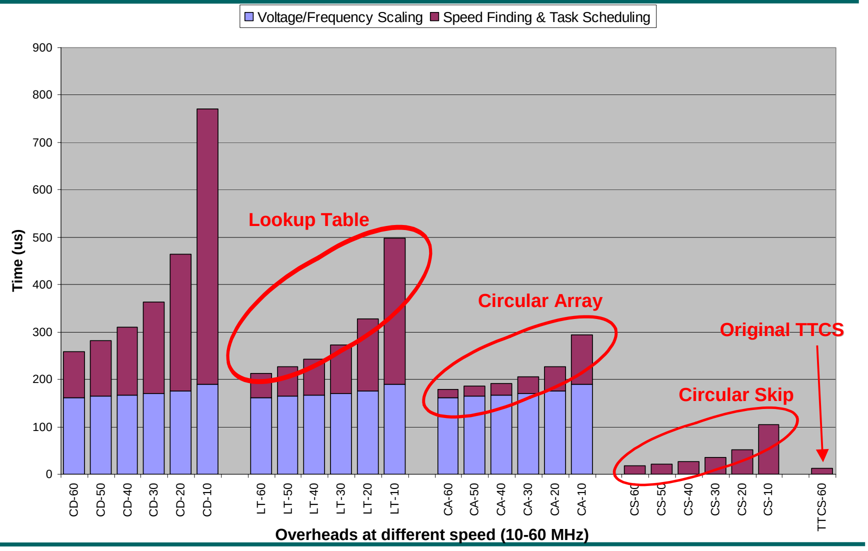
Overheads comparison



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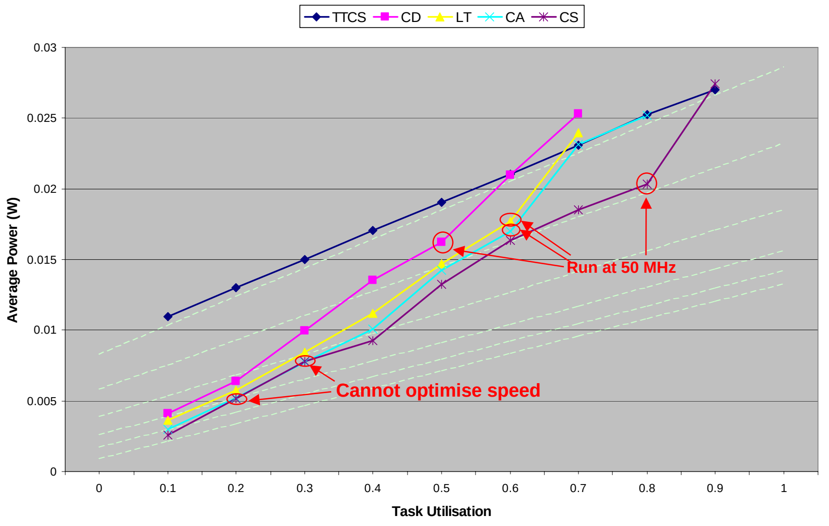
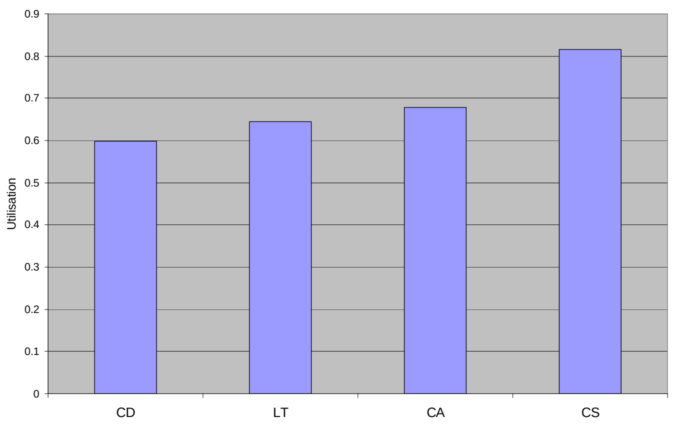
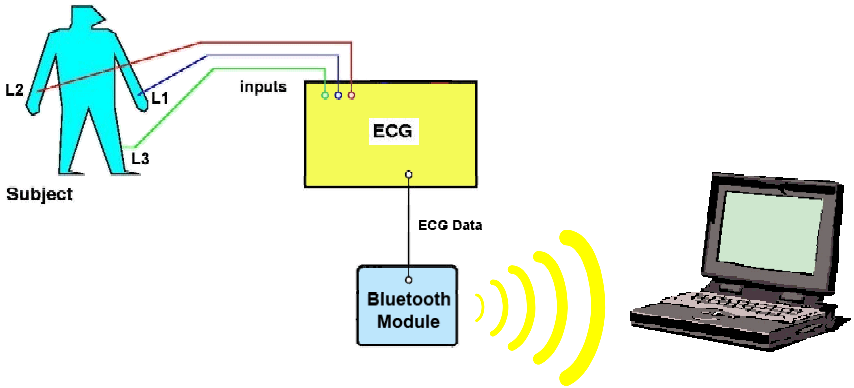
Power consumption comparison



Break-even points of the DVS algorithms

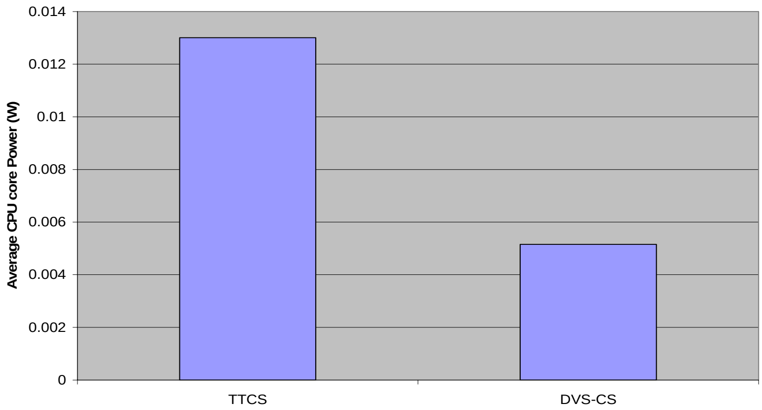


Case study: Wireless ECG



Phatrapornnant, T. and Pont, M.J. (2004) "The application of dynamic voltage scaling in embedded systems employing a TTCS software architecture: A case study", System-On-Chip Design, Test and Technology, Loughborough, UK.

Case study: Wireless ECG (2)



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Conclusions

- The application of DVS on TTCS has the potential to reduce CPU power consumption
- DVS-CS which has smallest overhead is the most power-efficient of the DVS algorithms considered here
- CPU power consumption on a wireless ECG system was reduced by about 60% when employing DVS-CS

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